ABSTRACT

A circuit to monitor the activity of a memory device during program/erase operations that are managed by a ROM-based microcontroller. Different signals can be monitored according to different test modes. The ROM-based microcontroller is triggered by a clock that can be connected to an internal fixed frequency oscillator or to an external clock source for which the frequency can be varied from 0 Hz to any frequency required by the application. The circuit outputs state machine status data, read only memory addresses, and memory status information in a series of multiplexing operations to provide a tester with the ability to determine the state of a memory device during various memory operations.